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TITLE: Computer segmented memory management technique wherein two expandable memory portions are contained within a single segment

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CLAIMS:

It is claimed:

1. In a computer system that includes a central processing unit characterized by specifying an address of one of a plurality of memory segments on a segment bus and a particular memory location within the designated memory segment on an address bus, a system for managing physical memory of said computer system, comprising:

first and second memory management units each having an input connected to said segment bus and to at least a most significant portion of the address bus, each of said memory management units being characterized by generating at an output connected to a memory a distinct stored physical memory segment starting address for at least one segment number received on said segment bus and generating an offset address within each of said physical segments according to the address of the address bus, each of said memory management units further being characterized by controlling the size of said at least one logical memory segment actually used in accordance with the damands of the system, said first memory management unit connected to operate from a lower end of said at least one logical memory segment and expand toward a higher end thereof, said second memory management until connected to operate from said higher end of said at least one logical memory segment and expand toward said lower end, and

means responsive to said address bus and connected to said first and second memory management units for enabling only one of said first and second memory management units at a time, said enabling means operating to enable said first memory management unit when the address carried by said address bus is on one side of a break value intermediate of said lower and said higher ends of said at least one logical memory segment, and to enable said second memory management unit when the address carried by said address bus is on the other side of said break value, whereby two variable size physical segments of memory can be controlled within a single logical memory segment.

2. The system according to claim 1, wherein said enabling means includes a register for storing the break value, said register being connected to the central processing unit in a manner that it may be updated by signals from the central processing unit to correspond to the changing logical memory size controlled by one of the first or second memory management units.

3. The system according to claim 1, wherein one of said first and second memory

management units is utilized to control stack memory and the other is used to control data memory.

4. The system according to claim 3, wherein said enabling means includes a register containing said break value, said register connected to the central processing unit in a manner to be updated by signals from the central processing unit in response to growth of the data memory.

5. A computer system, comprising:

a central processing unit having address bus terminals,

a random access memory having address bus terminals,

at least first and second memory management units, each of which is characterized by having input terminals adapted to receive logical memory addresses within at least a given segment of addresses with means therein for converting an address within said logical segment into a physical memory address within distinct physical address segments at output terminals thereof,

an address bus having a plurality of conductors, some of which are connected directly between said microprocessor bus terminals and said memory address bus terminals, others of which are connected between remaining central processing unit address terminals and said first and second memory management unit input terminals, and yet others of which are connected from the memory management unit output bus terminals to remaining of said memory address bus terminals, and

means responsive to an address on a plurality of said central processing unit address terminals for enabling either said first or said second memory management unit, but not both, depending upon whether the address is above or below a given break address that is within said given logical segment,

whereby said one logical memory segment is separately accessed through said first and second memory management units.

6. The system according to claim 5, wherein said enabling means comprises means for comparing an address on said plurality of central processing unit address terminals with an address maintained in a register.

7. The system according to claim 6, wherein said enabling means additionally comprises means responsive to a plurality of said central processing unit address bus terminals for updating said predetermined address within said break register.

8. The system according to claim 5 wherein said first memory management unit is connected to respond to addresses beginning at a lower address end of said given logical segment and expand toward a higher address end thereof, and wherein said second memory management unit is connected to respond to addresses beginning at said higher end of said given logical segment and expand toward the lower address end thereof, whereby the full extent of said given logical segment may be utilized on either side of said break address.

9. In a segmented memory computer system having a central processing unit capable of generating logical memory addresses at address bus terminals, an improved system for managing said memory, comprising an address bus means connected between said central processing unit terminals and address terminals of a random access memory and having means in the path of at least a portion of said bus for converting a logical memory address thereon into a physical memory address that is applied to said memory address terminals, said converting means being characterized by responding to logical addresses on one side of a dividing address within at least one given logical segment of addresses to generate a physical address in a first physical segment of addresses and by responding to logical addresses on another side of said dividing address within said given logical segment to generate a physical address in a second physical segment of addresses that is separate and distinct from the first physical segment, whereby said given logical address segment is divided into two distinct physical address segments.

10. The system according to claim 9, which additionally comprises means responsive to said logical addresses for adjusting said logical segment dividing address.

11. The system according to claim 9 wherein said converting means is additionally

characterized by responding to addresses on said one side of the dividing address beginning at a lower address end of said given logical segment and expanding toward said dividing address, and by responding to addresses on said another side of the dividing address beginning at a higher end of said given logical segment and expanding toward said dividing address, whereby the full extent of said given logical segment may be utilized on either side of said break address.